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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/054,972	01/25/2002	Yoshiyasu Doi	100021-00066	8817

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EXAMINER	
PERILLA, JASON M	

ART UNIT	PAPER NUMBER
2611	

DATE MAILED: 05/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/054,972	DOI ET AL.	
	Examiner	Art Unit	
	Jason M. Perilla	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 August 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-81* is/are pending in the application.

4a) Of the above claim(s) *2-4, 6-9, 11-13, 15-27, 29-31, 33-36, 38-40, 42-54, 56-58, 60-63, and 65-67* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,5,10,14,28,32,37,41,55,59,64 and 68* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-81 are pending in the instant application. Claims 2-4, 6-9, 11-13, 15-27, 29-31, 33-36, 38-40, 42-54, 56-58, 60-63, and 65-67 are withdrawn from further consideration.

Response to Arguments

2. Applicant's arguments filed March 13, 2006 have been fully considered but they are not persuasive. The Applicant has failed to address, substantively, the prior art rejections set forth in the first office action dates October 17, 2005. The Examiner points out that, as broadly as claimed, the prior art rejections meet all of the claim limitations as provided below.

3. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., the input voltages are not caused by a charge-sharing operation; see pg. 17, lines 18-19) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

4. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1, 10, 28 and 37 are rejected under 35 U.S.C. 102(b) as being anticipated by Early et al (US 5391999 – hereafter "Early").

Regarding claim 1, Early et al discloses according to figure 2 a receiver circuit comprising: a sampling circuit (43, 48) sampling an input signal (V_{INP}, V_{INM}); a buffer circuit (47) buffering an output of said sampling circuit; a determining circuit (69) determining an output of said buffer circuit; and a buffer control circuit (45, 46, 50 and 51) keeping a small input signal dependency of the output of said buffer circuit until (col. 10, lines 35-45) carrying out said sampling (fig. 5; col. 10, lines 4-15; col. 10, lines 44-53, ***54-58***). The differential switched-capacitor filter disclosed by Early receives a signal V_{IN}, samples the signal, buffers the signal, and determines, accordingly, an output signal V_{OUT}. The buffer circuit control circuit, which is comprised of various switched capacitors, is utilized to appropriately gate and charge or discharge voltage and current in the buffer to prevent glitches which result from the sampling and transitions of the input signal (col. 1, lines 20-35).

Regarding claim 10, the limitations of the claim are disclosed by Early as applied to claim 1 above. Further, Early disclose that the buffer control circuit is a buffer control circuit substantially constant value of the output of said buffer circuit until carrying out said sampling. According to figure 2, the buffer circuit (47) is kept constant by the buffer

control circuit because the buffer control circuit either clamps (46 or 51) the input to the buffer via control signal φ1 (fig. 5) when sampling is about to occur via sampling clock φ1D (fig. 5) or passes (45, 50) the sampled signal via control signal φ2 (fig. 5) once sampling has occurred.

Regarding claim 28, Early discloses the limitations of the claim as applied to claim 1 above.

Regarding claim 37, Early discloses the limitations of the claim as applied to claim 10 above.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 5, 14, 32, 41, 55, 59, 64, and 68 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawabata (US 6452518) in view of Early.

Regarding claim 5, Kawabata teaches a bit interleaving apparatus according to figure 3A, wherein two sampling or receiving circuits (13a and 13b) are used with two phase offset clock signals (52a and 52b) to effectively double the sampling data rate of a signal (50) which allows two times as much data to be transmitted (col. 1, lines 54-65) using sampling units that run at half the full data rate. Kawabata does not disclose that the sampling or receiving circuits (13a and 13b) are receiver circuits as provided in claim 1. However, Early teaches receivers having sampling circuits which disclose the

limitations of claim 1 as applied above. Further, Early teaches that the receivers are advantageous because the buffer control circuits of the receivers prevent switching "glitches" from being induced in the outputs (col. 1, lines 20-35). Therefore, it would have been obvious to one having skill in the art at the time which the invention was made to replace the samplers or receivers of Kawabata with the receivers of Early (i.e. fig. 2 embodiment) because each of the receivers of Early is specifically designed to prevent switching glitches from propagating. Further, the Examiner notes and concedes that the analog to digital converters of Kawabata (13a and 13b) are not strictly analogous to the all digital receivers and buffers of Early. Nonetheless, one skilled in the art is still motivated to utilize the advantage of Kawabata's data interleaving in an all digital context as combined with Early's receivers. Hence, the combination of Kawabata in view of Early comprises a plurality of sample switches sampling a series of bits, and a plurality of said buffer circuits corresponding to said sample switches are provided.

Regarding claim 14, Kawabata teaches a bit interleaving apparatus according to figure 3A, wherein two sampling or receiving circuits (13a and 13b) are used with two phase offset clock signals (52a and 52b) to effectively double the sampling data rate of a signal (50) which allows two times as much data to be transmitted (col. 1, lines 54-65) using sampling units that run at half the full data rate. Kawabata does not disclose that the sampling or receiving circuits (13a and 13b) are receiver circuits as provided in claim 10. However, Early teaches receivers having sampling circuits which disclose the limitations of claim 10 as applied above. Further, Early teaches that the receivers are advantageous because the buffer control circuits of the receivers prevent switching

"glitches" from being induced in the outputs (col. 1, lines 20-35). Therefore, it would have been obvious to one having skill in the art at the time which the invention was made to replace the samplers or receivers of Kawabata with the receivers of Early (i.e. fig. 2 embodiment) because each of the receivers of Early is specifically designed to prevent switching glitches from propagating. Further, the Examiner notes and concedes that the analog to digital converters of Kawabata (13a and 13b) are not strictly analogous to the all digital receivers and buffers of Early. Nonetheless, one skilled in the art is still motivated to utilize the advantage of Kawabata's data interleaving in an all digital context as combined with Early's receivers. Hence, the combination of Kawabata in view of Early comprises a plurality of sample switches sampling a series of bits, and a plurality of said buffer circuits corresponding to said sample switches are provided.

Regarding claim 32, Kawabata in view of Early disclose the limitations of the claim as applied to claim 5 above.

Regarding claim 41, Kawabata in view of Early disclose the limitations of the claim as applied to claim 14 above.

Regarding claim 55, Kawabata teaches a bit interleaving apparatus according to figure 3A, wherein two sampling or receiving circuits (13a and 13b) are used in a interleaved fashion with two phase offset clock signals (52a and 52b) to effectively double the sampling data rate of a signal (50) which allows two times as much data to be transmitted (col. 1, lines 54-65) using sampling units that run at half the full data rate. Kawabata does not disclose that the sampling or receiving circuits (13a and 13b) are receiver circuits as provided in claim 1. However, Early teaches receivers having

sampling circuits which disclose the limitations of claim 1 as applied above. Further, Early teaches that the receivers are advantageous because the buffer control circuits of the receivers prevent switching "glitches" from being induced in the outputs (col. 1, lines 20-35). Therefore, it would have been obvious to one having skill in the art at the time which the invention was made to replace the samplers or receivers of Kawabata with the receivers of Early (i.e. fig. 2 embodiment) because each of the receivers of Early is specifically designed to prevent switching glitches from propagating. Further, the Examiner notes and concedes that the analog to digital converters of Kawabata (13a and 13b) are not strictly analogous to the all digital receivers and buffers of Early. Nonetheless, one skilled in the art is still motivated to utilize the advantage of Kawabata's data interleaving in an all digital context as combined with Early's receivers.

Regarding claim 59, Kawabata in view of Early disclose the limitations of claim 55 as applied above. Further, in the circuit of Kawabata in view of Early, a plurality of receiver units are operated in an interleaved fashion. Hence, the combination of Kawabata in view of Early comprises a plurality of sample switches (a pair for each receiver) sampling a series of bits, and a plurality of said buffer circuits (one for each receiver) corresponding to said sample switches are provided.

Regarding claim 64, Kawabata teaches a bit interleaving apparatus according to figure 3A, wherein two sampling or receiving circuits (13a and 13b) are used in a interleaved fashion with two phase offset clock signals (52a and 52b) to effectively double the sampling data rate of a signal (50) which allows two times as much data to be transmitted (col. 1, lines 54-65) using sampling units that run at half the full data rate.

Kawabata does not disclose that the sampling or receiving circuits (13a and 13b) are receiver circuits as provided in claim 1. However, Early teaches receivers having sampling circuits which disclose the limitations of claim 10 as applied above. Further, Early teaches that the receivers are advantageous because the buffer control circuits of the receivers prevent switching "glitches" from being induced in the outputs (col. 1, lines 20-35). Therefore, it would have been obvious to one having skill in the art at the time which the invention was made to replace the samplers or receivers of Kawabata with the receivers of Early (i.e. fig. 2 embodiment) because each of the receivers of Early is specifically designed to prevent switching glitches from propagating. Further, the Examiner notes and concedes that the analog to digital converters of Kawabata (13a and 13b) are not strictly analogous to the all digital receivers and buffers of Early. Nonetheless, one skilled in the art is still motivated to utilize the advantage of Kawabata's data interleaving in an all digital context as combined with Early's receivers.

Regarding claim 68, Kawabata in view of Early disclose the limitations of claim 64 as applied above. Further, in the circuit of Kawabata in view of Early, a plurality of receiver units are operated in an interleaved fashion. Hence, the combination of Kawabata in view of Early comprises a plurality of sample switches (a pair for each receiver) sampling a series of bits, and a plurality of said buffer circuits (one for each receiver) corresponding to said sample switches are provided.

Allowable Subject Matter

9. No claims are allowed.

Conclusion

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason M. Perilla whose telephone number is (571) 272-3055. The examiner can normally be reached on M-F 8-5 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh M. Fan can be reached on (571) 272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jason M. Perilla
May 9, 2006

jmp

CHIEH M. FAN
SUPERVISORY PATENT EXAMINER